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10EC63

Sixth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Micro Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the following parameters with respect to MOSFET:
i) Threshold voltage; ii) Overdrive voltage. **(05 Marks)**

b. Explain the breakdown effect occurs in MOSFET. **(05 Marks)**

c. Draw the biasing circuit using a drain to gate feedback resistor and explain it. **(05 Marks)**

d. For the circuit shown in Fig.Q.1(d), find the values of R and V_D to obtain a current I_D of 80μA. Let the NMOS transistor have $V_t = 0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $L = 0.8\ \mu m$ and $W = 4\ \mu m$. Assume $\lambda = 0$. **(05 Marks)**

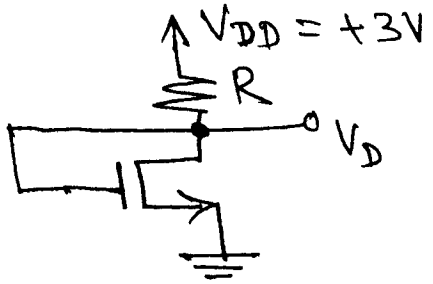

Fig.Q.1(d)

2 a. What are the disadvantages due to short-channel effects? **(05 Marks)**

b. The high frequency response of an amplifier is characterized by the TF

$$F_H(s) = \frac{1-\frac{s}{10^5}}{\left(1+\frac{s}{10^4}\right)\left(1+\frac{s}{4\times10^4}\right)}$$. Determine the 3-dB frequency. **(05 Marks)**

c. What is current steering? Mention its advantages. **(05 Marks)**

d. Draw the circuit of basic MOSFET current source and explain it. **(05 Marks)**

3 a. Draw the circuit and small signal equivalent circuit of common source amplifier with active load and explain it. **(06 Marks)**

b. What is cascade amplifier and mention the basic idea behind the cascade amplifier? **(06 Marks)**

c. Draw the circuit of double cascading and explain it. **(08 Marks)**

4 a. Draw the transistor pairing circuits and mention the advantages of each pair. **(06 Marks)**

b. Draw the circuit of cascade MOS current mirror and explain it. **(06 Marks)**

c. Explain the operation of a MOS differential pair with a common mode input voltage and mention the relevant equations. **(08 Marks)**

PART – B

5 a. The differential amplifier shown in Fig.Q.5(a) uses transistors with $\beta = 100$. Evaluate:
   i) Input differential resistance (R_{id}).
   ii) Overall differential voltage gain V_o/V_{sig} (neglect the effect of V_o).
   iii) CMRR in dB. (Assume $A_{cm} = 5 \times 10^{-4}$).
   iv) Input common mode resistance (assuming that the early voltage $V_A = 100V$. **(10 Marks)**

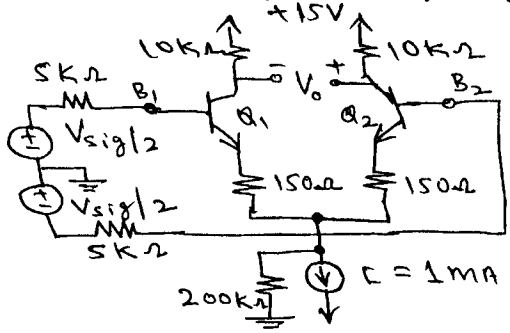

Fig.Q.5(a)

   b. Draw the two-stage CMOS Op-Amp circuit and explain it. **(10 Marks)**

6 a. Explain the properties of negative feedback. **(10 Marks)**
   b. Explain the effect of feedback on the amplifier stability and pole location. **(07 Marks)**
   c. What are the properties of current amplifier? **(03 Marks)**

7 a. Derive the expression for the closed loop gain V_o/V_{in} of the circuit shown in Fig.Q.7(a). **(08 Marks)**

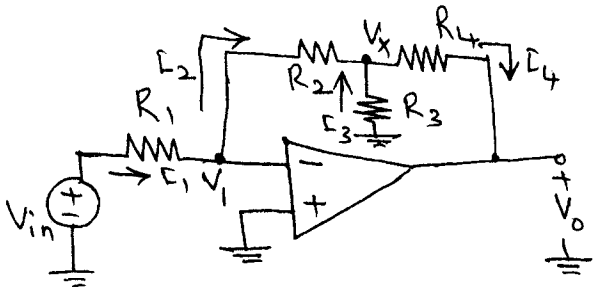

Fig.Q.7(a)

   b. With the help of mathematical analysis, explain how to minimize the temperature effect in logarithmic amplifier. **(10 Marks)**
   c. What are DC imperfections? **(02 Marks)**

8 a. Obtain the PUN from the PDN and vice versa for the following expressions:
   i) $Y = \overline{A(B+CD)}$ ii) $Y = \overline{A(B+AC)}$ **(12 Marks)**
   b. Define the following parameters with respect to CMOS:
   i) Propagation delay
   ii) Robustness
   iii) Delay power product
   iv) Dynamic power dissipation. **(08 Marks)**

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